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# SOLID-STATE IMAGING ELEMENT, IMAGE PROCESSOR AND IMAGE PROCESSING METHOD

## BACKGROUND OF THE INVENTION

### Field of the Invention

The present invention relates to a solid-state imaging element for inputting optical image data and then converting this data into an electrical signal, and an image input device using this same solid-state imaging element.

### Description of the Related Art

In an image input device such as a digital camera, as illustrated in Fig. 1, optical image data transmitted through a lens 2 are input to a CCD (Charge Coupled Device) 4, which is a solid-state imaging element. In the CCD 4, the input image data are converted to an electrical signal, that is, to analog image data. The analog image data are converted to digital image data by an A/D converter 6 and the digital image data are stored in a frame memory 8. The digital image data stored in the frame memory 8 are then supplied to an image data encoder 10 comprising, for example, a discrete cosine transform (DCT) converting unit 12, a quantizing unit 14, and a Huffman encoding unit 16, or the like, and the image data are compressed through the encoding process.

As illustrated in Fig. 2, CCD 4 comprises a horizontal CCD section 30 and a vertical CCD section 32. In the vertical CCD section 32, photosensors 34, such as photodiodes, are

arranged such that the photosensors 34 correspond to the pixels of a frame image. Each photosensor 34 receives the images corresponding to one pixel and converts an optical beam into a voltage to generate analog image data.

The horizontal CCD section 30 includes line buffers for outputting the analog image data. The analog image data corresponding to one pixel generated in each photosensor 34, are shifted stage by stage in the vertical direction (from a to b) and are then input to the line buffer that holds the analog image data of one line. The line buffer holding the analog image data of one line, shifts the analog image data one-by-one in the horizontal direction (from c to d) and outputs the data to an external circuit of the CCD 4. The analog image data output from the CCD 4 are then input to an A/D converter 6. The analog image data are converted to digital image data by the A/D converter 6 and then transferred to the image data encoder 10 and compressed through the encoding process.

In the image data encoder 10, the image data are divided and processed in predetermined units (hereinafter, referred to as blocks). As illustrated in Fig. 3A, for example, in JPEG image encoding, the image data are encoded as an 8x8 array or block of pixels. In each block, the image data are often processed in a sequence from upper left to lower right, as illustrated in Fig. 3B.

In Fig. 4, one block 52 comprises an 8x8 array of pixels (refer to Fig. 3A). As illustrated in Fig. 4, the image data of one frame 50 (the layout of the image data is identical to the layout in the vertical CCD 32) are divided into n blocks, and the encoding process is executed in the sequence 1, 2,..., n.

In the CCD 4, the image data of one frame 50 are output for each line as illustrated in Fig. 2. Meanwhile, in the image data encoder 10, which receives the data from the CCD 4 and then encodes the data, the encoding process is performed in predetermined units of a block as illustrated in Fig. 4. Therefore, the image data output from the CCD 4 must be rearranged to a layout suitable for the encoding process. Rearrangement may be conducted by the operations explained below.

(1) Operation using RAM:

In the first approach, as illustrated in Fig. 5, the image data output from the CCD 4 are written into RAM 70 and input to the image data encoder 10 via the RAM 70. When executing the encoding process in the image data encoder 10, address conversion is conducted and the data are read in the sequence required for the encoding process.

(2) Operation using line buffers:

In the second approach, as illustrated in Fig. 6A, the image data output from the CCD 4 are input to the image data encoder 10 via an 8-line buffer 90 (or a 16-line buffer in the case of a double buffer). As illustrated in Fig. 6B, the data of an 8-line CCD 4 are read into the line buffer 90. As illustrated in Fig. 6C, data are read in units of 8 pixels from the line buffer 90.

However, reading data using the rearrangement processes explained above has the following problems.

First, RAM is expensive and occupies a large area. Therefore, the number of RAMs used must be controlled. Often, only one RAM is used in common for various purposes. In

this case, when a RAM is used for only one purpose, application to other purposes is prevented. Accordingly, access control for multiple applications is rather complicated. Moreover, when a single RAM is being used for other applications, image data cannot be read. Therefore, it is impossible to realize a high-speed encoding process for image data. In addition, address conversion is complicated.

Second, line buffers must be prepared for reading image data. Because a line buffer is used exclusively for one operation, it cannot be used in common with another operation.

## SUMMARY OF THE INVENTION

In view of the above, the present invention provides a solid-state imaging element comprising a plurality of light receiving sensors for converting optical image data into electrical signals and a memory for storing the electrical signals, wherein the memory contains a plurality of line buffers.

In particular, the solid-state imaging element comprises a plurality of L (L is a positive integer) light receiving sensors arranged in one line for converting optical image data into an electrical signal and a memory for storing the electrical signal, wherein the memory contains a plurality of buffers, each holding m pixels of data. An image processor having such a solid-state image element is also provided.

According to the solid-state imaging element and image processor of the present invention, the image data output from a CCD 4 can be provided, without being rearranged, to an image data encoder 10, eliminating the need for a RAM or an exclusive line buffer for

rearranging image data. Therefore the transfer process may be simplified, the physical size of the circuit structure may be reduced, and high-speed image data transfer may be realized.

These together with other objects and advantages that will be subsequently apparent, reside in the details of construction and operation as more fully hereinafter described and claimed, reference being had to the accompanying drawings forming a part hereof, wherein like numerals refer to like parts throughout.

## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of an image input device.

Fig. 2 is a diagram of a CCD.

Fig. 3A is a diagram of image data for an 8x8 block of pixels.

Fig. 3B is a diagram of the sequence of processing for the image data of Fig. 3A.

Fig. 4 is a diagram of image data for one frame.

Fig. 5 is a diagram showing the use of RAM in the rearrangement of image data.

Fig. 6A is a diagram showing the use of a line buffer in the rearrangement of image data.

Fig. 6B is also a diagram showing the use of a line buffer in the rearrangement of image data.

Fig. 6C is another diagram showing the use of a line buffer in the rearrangement of image data.

Fig. 7 is a diagram of a first embodiment of the present invention.

Fig. 8A is a diagram of a vertical CCD.

Fig. 8B is a diagram of a vertical CCD and line buffers.

Fig. 9 is a diagram of a first switch circuit and a first switch control circuit.

Fig. 10 is a diagram of a timing chart for the vertical direction transfer period.

Fig. 11 is a diagram of a second switch circuit and a second switch control circuit.

Fig. 12 is a diagram of a timing chart for the horizontal direction transfer period.

Fig. 13 is a diagram of a second embodiment of the present invention.

Fig. 14 is a diagram of a transfer control circuit.

Fig. 15 is a diagram of another timing chart for the vertical direction transfer period.

Fig. 16 is a diagram of a third embodiment of the present invention.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 7 is a diagram of a first embodiment of the present invention. The CCD 4 of Fig. 7 comprises, like the CCD 4 of Fig. 2, a horizontal CCD 30 and a vertical CCD 32. However, the horizontal CCD 30 illustrated in Fig. 7 comprises a number of line buffers corresponding to the number of horizontal lines required for image data processing. For example, n line buffers are provided for image data that are encoded in the image data encoder 10 in an n x m block (vertical x horizontal) of pixels.

The CCD 4 illustrated in Fig. 7 also comprises a first switch circuit 100, a second switch circuit 102, a first switch control circuit 104, and a second switch control circuit 106. The first switch circuit 100 connects to each vertical line of the vertical CCD 32. The first

switch control circuit 104 controls the first switch circuit 100 so that only one of the plurality of line buffers of the horizontal CCD 30 connects to the vertical CCD 32. The second switch control circuit 106 controls the second switch circuit 102 so that only one of the plurality of line buffers of the horizontal CCD 30 connects to an external circuit (not illustrated).

The operation for outputting image data from the CCD 4 illustrated in Fig. 7 is explained below with reference to Figs. 8A and 8B. In the embodiment shown in Fig. 8A, 100 pixels are contained in a 10x10 array of image data. Figs. 8A and 8B illustrate an example of how image data are stored in the vertical CCD 32 and the line buffers 120-124. In Figs. 8A and 8B, it is assumed that the image data encoder 10 performs the encoding process on units of 3x2 blocks (vertical x horizontal) of pixel data. Therefore, three line buffers are used.

The image data are first transferred in the vertical direction. The first switch control circuit 104 controls the first switch circuit 100 to connect the first line buffer 120 and the vertical CCD 32. The image data corresponding to one horizontal line are transferred to the first line buffer 120 from the vertical CCD 32. Next, the first switch control circuit 104 controls the first switch circuit 100 to connect the second line buffer 122 and the vertical CCD 32. The image data of the next horizontal line are transferred to the second line buffer 122 from the vertical CCD 32. As explained above, the first switch control circuit 104 switches the connections of the first switch circuit 100 until all the line buffers are filled with image data.

The image data corresponding to three horizontal lines are transferred to the line buffers, from the vertical CCD 32 shown in Fig. 8A. Fig 8B illustrates the condition where all the buffers are filled with the image data of vertical CCD 32.

Next, the image data are transferred in the horizontal direction. Transfer in the horizontal direction is performed after the image data are supplied to all of the n line buffers. The second switch control circuit 106 controls the second switch circuit 102 to connect the first line buffer 120 and an external circuit of the CCD 4. The image data of m pixels are output to the external circuit of the CCD 4 from the first line buffer 120. Next, the second switch control circuit 106 controls the second switch circuit 102 to connect the second line buffer 122 and the external circuit of the CCD 4. The image data of m pixels are output to the external circuit of the CCD 4 from the second line buffer 122. The image data of n line buffers are output to the external circuit of the CCD 4 by repeating similar output operations.

Fig. 8B is explained in more detail below. The second switch control circuit 106 controls the second switch circuit 102 to connect the first line buffer 120 and the external circuit of the CCD 4. The first line buffer 120 outputs the image data (pixels 1 and 2) to the external circuit of the CCD 4. Next, the second switch control circuit 106 controls the second switch circuit 102 to connect the second line buffer 122 and the external circuit of the CCD 4. The second line buffer 122 outputs the image data (pixels 11 and 12) to the external circuit of the CCD 4. Then, the second switch control circuit 106 controls the second switch circuit 102 to connect the third line buffer 124 to the external circuit of the CCD 4. The

third line buffer 124 outputs the image data (pixels 21 and 22) to the external circuit of the CCD 4. As explained above, this results in output of the image data of block 1. By repeating similar output operations, the image data of block 1 to block 5 are sequentially output.

By repeating transfer in the vertical and horizontal directions, the image data of one frame are output completely. That is, the image data from the first to the one-hundredth pixel of the vertical CCD 32 of Fig. 8A are all output.

Fig. 9 is a circuit diagram of the first switch circuit 100 and the first switch control circuit 104. The first switch circuit 100 connects one vertical line of the vertical CCD 32 and the storage area of one line buffer (hereinafter referred to as "storage area"). This first switch circuit 100 connects to each vertical line of the vertical CCD 32. In Fig. 9, it is assumed that the first switch circuit 100 connects to the first vertical line of the vertical CCD 32. A switch S11 connects the first vertical line of the vertical CCD 32 and the first storage area of the first line buffer 120. A switch S12 connects the first vertical line of the vertical CCD 32 and the first storage area of the second line buffer 122. A switch S1n connects the first vertical line of the vertical CCD 32 and the first storage area of the nth line buffer 126.

The switches S1 to S1n are controlled by the first switch control circuit 104. The first switch control circuit 104 comprises a shift register having n flip-flop (FF) circuits. An output SW11 of the first flip-flop F11 controls the ON/OFF condition of the switch S11. An output SW12 of the second flip-flop F12 controls the ON/OFF condition of the switch S12. An output SW1n of the nth flip-flop F1n controls the ON/OFF condition of the switch S1n.

A reset signal $V_{reset}$ is input to the flip-flops F11 to F1n to initialize the flip-flop circuits. The flip-flop F11 is initialized with the signal "1", while the other flip-flop circuits are initialized with the signal "0". Also, a vertical direction shift pulse $V_{CLK}$ is supplied to the flip-flop circuits F11 to F1n.

Fig. 10 is a timing chart illustrating the operations of the first switch circuit 100 and first switch control circuit 104 of Fig. 9 during the transfer in the vertical direction. A first shift pulse occurs when the flip-flop F11, initialized with the signal "1", outputs a "1" for control signal SW11. The other flip-flop circuits, initialized with the signal "0", output a "0" for the control signals SW12 to SW1n. Therefore, the switch S11 turns ON to transfer the image data of the first horizontal line of the vertical CCD 32 to the storage area of the first line buffer 120. Each flip-flop receives the signal output from the preceding flip-flop circuit.

A second shift pulse occurs when the flip-flop F12, having received the output signal "1" from the flip-flop F11, outputs a "1" for the control signal SW12. The other flip-flop circuits that have received the output signal "0" from the flip-flop of the preceding stage output a "0" for the control signal SW11 and the control signals SW13 to SW1n. Therefore, the switch S12 turns ON to transfer the image data of the second horizontal line of the vertical CCD 32 to the storage area of the second line buffer 122. Each flip-flop again receives the signal output from the preceding flip-flop. When the third shift pulse occurs, a third switch turns ON to transfer the image data of the third horizontal line of the vertical CCD 32 to the storage area of the third line buffer 124.

The operations above are repeated for n shift pulses and the image data for n horizontal lines of the vertical CCD 32 are stored in the n line buffers. Thereafter, the horizontal transfer period occurs to transfer the image data from the line buffers to the external circuit of the CCD 4. During the horizontal transfer period, shift pulses in the vertical direction are not present.

Fig. 11 is a circuit diagram of the second switch circuit 102 and the second switch control circuit 106. The second switch circuit 102 connects one of the line buffers of the horizontal CCD 30 and the external circuit. The switch S21 connects the first line buffer 120 and the external circuit. The switch S22 connects the second line buffer 122 and the external circuit. The switch S2n connects the nth line buffer 126 and the external circuit.

The switches S21 to S2n are controlled by the second switch control circuit 106. The second switch control circuit 106 comprises a shift register having n flip-flop (FF) circuits and a counter 130. An output SW21 of the first flip-flop F21 controls the ON/OFF condition of the switch S21. An output SW22 of the second flip-flop F22 controls the ON/OFF condition of the switch S22. An output SW2n of the nth flip-flop F2n controls the ON/OFF condition of the switch S2n.

The reset signal $H_{reset}$ is input to the flip-flop circuits F21 to F2n for initialization. The flip-flop F21 is initialized with the signal "1", while the other flip-flops are initialized with the signal "0". Also, the horizontal direction shift pulse $H_{CLK}$ is input to the flip-flop circuits F21 to F2n. The horizontal direction shift pulse $H_{CLK}$ is input to the counter 130.

The counter 130 counts the number of horizontal direction shift pulses $H_{CLK}$ (up to m pulses) and supplies the enable signal EN to the flip-flop F2n beginning with the flip-flop F21.

Fig. 12 is a timing chart of the operations during the transfer period in the horizontal direction for the second switch circuit 102 and second switch control circuit 106 of Fig. 9. When the counter 130 provides the first enable signal, the flip-flop F21, initialized with the signal "1", outputs a "1" for the control signal SW21. The other flip-flop circuits, initialized with the signal "0", output a "0" for the control signal SW22 to the control signal SW2n. Therefore, the switch S21 turns ON to output the image data of the first line buffer 120 to the external circuit.

Each flop-flop receives the signal output from the preceding flip-flop. Thereafter, the counter 130 is reset and does not provide the enable signal to the flip-flops until the horizontal direction pulse signal is counted for m times.

When the counter 130 provides the second enable signal, the flip-flop F22, having received the output signal "1" from the flip-flop F21, outputs a "1" for the control signal SW22. The other flip-flop circuits, having received the output signal "0" from the flip-flop in the preceding stage, output a "0" for the control signal SW21 and the control signal SW23 to the control signal SW2n. Therefore, the switch S22 turns ON to output the image data of the second line buffer 122 to the external circuit.

Each flip-flop again receives the signal output from the preceding flip-flop. Thereafter, the counter 130 is reset and does not supply the enable signal to the flip-flops until the horizontal direction shift pulse $H_{CLK}$ is counted m times. When the counter 130

provides the third enable signal, a third switch turns ON to output the image data of the third line buffer 124 to the external circuit.

The operations above are repeated until the image data of the line buffers are completely output to the external circuit. Thereafter, the period to transfer the image data to the line buffers in the vertical direction from the vertical CCD 32 begins. During the vertical transfer period, the horizontal shift pulses $H_{CLK}$ are not present.

According to the first embodiment of the present invention illustrated in Fig. 7, the image data are sequentially output in units of m pixels from the n line buffers holding the image data. In other words, the image data are output from the CCD 4 in the form obtained by dividing one frame into units of blocks of n x m pixels. Therefore, the output image data may be provided to the image data encoder 10 without being rearranged.

Fig. 13 is a diagram of a second embodiment of the present invention. The CCD 4 illustrated in Fig. 13 comprises, like the CCD 4 illustrated in Fig. 2, a horizontal CCD 30 and a vertical CCD 32. However, the horizontal CCD 30 illustrated in Fig. 13 divides a single line into a plurality of sections and comprises a number of buffers equal to the number of line sections. That is, where the image data are encoded in the image data encoder 10 in blocks of n x m (vertical x horizontal) pixels, the number of buffers (hereinafter, "buffer number" or "k") is determined by dividing the number of pixels in a horizontal line by m. Here, one buffer is capable of storing the image data corresponding to m pixels.

The CCD 4 illustrated in Fig. 13 also comprises a third switch circuit 140, a third switch control circuit 142, and a transfer control circuit 144. The third switch control

circuit 142 controls the third switch circuit 140 to connect only one of the plurality of buffers of the horizontal CCD 30 and an external circuit (not illustrated). The transfer control circuit 144 controls the vertical CCD 32 to provide the image data to the buffers connected to the external circuit.

Operations for outputting the image data of the CCD 4 shown in Fig. 13 are explained below. The third switch control circuit 142 controls the third switch circuit 140 to connect the first buffer 146 and the external circuit. The transfer control circuit 144 controls the vertical CCD 32 to transfer the image data corresponding to the first buffer 146, that is, the image data of the first m pixels of the first horizontal line. The first buffer 146 outputs the image data to the external circuit. Next, the image data of the first m pixels of the second horizontal line are transferred to the first buffer 146 from the vertical CCD 32 and the first buffer 146 outputs the transferred image data to the external circuit. This process is repeated n times. Selection of the buffer and the vertical and horizontal transfers are repeated m times.

The third switch circuit 140 and the third switch control circuit 142 have circuit structures that are almost identical to the second switch circuit 102 and the second switch control circuit 106 of Fig. 11. The counter 160 of the third switch control circuit 142 counts the number of horizontal shift pulses $H_{CLK}$ (up to m pulses) and supplies the pulse signals to the flip-flops.

Fig. 14 is a circuit diagram of the transfer control circuit 144. The transfer control circuit 144 controls the vertical CCD 32 to supply the image data to the buffer connected to

the external circuit. The transfer control circuit 144 comprises a shift register with a number of flip-flop circuits equal to the number of buffers k, a number of AND gates equal to the number of buffers k, and a counter 160.

A signal output from each flip-flop circuit is provided to an input of a corresponding AND gate. A vertical shift pulse $V_{CLK}$ is also input to each AND gate. For example, the first AND gate G1 receives a signal output from the first flip-flop F31, and an output signal from the AND gate G1 controls transfer of the image data to the first buffer 146. An output of the second AND gate G2, which received an output from the second flip-flop F32, controls transfer of image data to the second buffer 148. An output of the kth AND gate Gk, which received an output from the flip-flop F3k, controls transfer of the image data to the kth buffer 150.

The reset signal $V_{reset}$ is supplied to the flip-flop F3k from the flip-flop F31 for initialization. The flip-flop F31 is initialized with the signal "1" and the other flip-flop circuits are initialized with the signal "0". Also, the enable signal EN of the counter 160 is input to the flip-flop F3k from the flip-flop F31. The counter 160 counts the number of vertical direction shift pulses $V_{CLK}$ (up to n times) and supplies the enable signal EN to the flip-flop F3k beginning with the flip-flop F31.

Fig. 15 is a timing chart of the operation of the transfer control circuit 144 of Fig. 14, that is, the transfer in the vertical and horizontal directions. When the counter 160 provides the first enable signal, the flip-flop F31, initialized with the signal "1", outputs the signal "1". The other flip-flop circuits, initialized with the signal "0", output the control

signal "0". The signal "1" output from the flip-flop F31 is then input to the AND gate G1. The other flip-flop circuits provide the signal "0" to one input of a corresponding AND gate. Therefore, only the AND gate G1 corresponding to the flip-flop F31 outputs the transfer pulse to the first buffer 146, and an output of each AND gate corresponding to the other flip-flop circuits, that is, the transfer pulses from the second buffers are not considered objects to the transfer operation.

The first buffer 146 performs the transfer operation based upon the vertical direction shift pulse $V_{CLK}$. When the vertical direction shift pulse $V_{CLK}$ is high, that is, when it is a "1", the image data are supplied to the first buffer 146 from the vertical CCD 32. When the vertical direction shift pulse $V_{CLK}$ is low, that is, when it is a "0", the m-pixel image data are supplied to the external circuit from the first buffer 146. Transfer of the image data to the first buffer 146 and output of the image data to the external circuit occur n times. In other words, the input and output of m pixels to and from the first buffer 146 is repeated a total of n times.

On the basis of the first enable signal from the counter 160, each flip-flop receives the signal output from the preceding flip-flop. Thereafter, the counter 160 is reset and the first enable signal is not generated for the flip-flops until the vertical direction shift pulse $V_{CLK}$ is counted n times.

When the counter provides the second enable signal, the flip-flop F32 receives the output signal "1" from the flip-flop F31 outputs the signal "1". The other flip-flop circuits receive the output signal "0" from the flip-flop in the preceding stage and output the signal

"0". Therefore, only the output of the AND gate G2 corresponding to the flip-flop F32 outputs the transfer pulse to the second buffer 148, and the output of each AND gate corresponding to the other flip-flop circuits is fixed to "0". Therefore, the transfer operation is performed only on the second buffer 148, and the transfer operation is not performed on any other buffers until the counter 160 outputs the third enable signal. Input and output of m pixels to and from the second buffer 148 is repeated a total of n times. When the counter 160 provides the third enable signal, the transfer operation is performed on the third buffer and so forth. These processes are repeated for each of the k buffers. Input and output of m pixels to and from the kth buffer is repeated a total of n times.

According to the second embodiment of the present invention shown in Fig. 13, up to n lines of image data may be sequentially output from each buffer holding image data of m pixels. That is, the image data are output from the CCD 4 in the units of blocks of n x m pixels of one frame. Therefore, the image data are supplied to the image data encoder 10 without needing to be rearranged.

Fig. 16 is a diagram of a third embodiment of the present invention. The CCD 4 illustrated in Fig. 16 comprises, like the CCD 4 illustrated in Fig. 2, a horizontal CCD 30 and a vertical CCD 32. However, the horizontal CCD 30 illustrated in Fig. 16 has as many line buffers as the number of lines required for the image data encoding process. That is, n line buffers are provided when encoding image data in the image data encoder 10 in blocks of n x m pixels.

The CCD 4 illustrated in Fig. 16 also comprises a fourth switch circuit 170 and a fourth switch control circuit 172. The fourth switch control circuit 172 controls the fourth switch circuit 170 so that only one of the plurality of line buffers of the horizontal CCD 30 connects to the vertical CCD 32.

The image data output operation of the CCD 4 illustrated in Fig. 16 is explained below. The fourth switch control circuit 172 controls the fourth switch circuit 170 to connect the first line buffer and the vertical CCD 32. The image data of one horizontal line are transferred to the first line buffer in the vertical direction from the vertical CCD 32. Next, the fourth switch control circuit 172 controls the fourth switch circuit 170 to connect the second line buffer and the vertical CCD 32. The image data of one horizontal line are transferred to the second line buffer from the vertical CCD 32. As explained above, the fourth switch control circuit 172 switches connections of the fourth switch circuit 170 to fill all line buffers with the image data.

Transfer in the horizontal direction is then performed after the image data are completely transferred to all of the n line buffers. The image data in the n line bluffers are output in parallel from the n line buffers. The transfer in the vertical direction and the transfer in the horizontal direction are repeated until the image data of one frame are completely output.

The fourth switch circuit 170 and the fourth switch control circuit 172 have the same circuit structures as the first switch circuit 100 and the first switch control circuit 104 of Fig. 9.

According to the third embodiment of the present invention shown in Fig. 16, the n lines of image data are output from the CCD 4 in parallel from the n line buffers holding the image

data in units of n x m pixels of one frame. In other words, the image data are output from the CCD 4 in units of n x m pixels until a plurality of n x m pixels yields one frame Therefore, the image data may be transferred to the image data encoder 10 without rearranging the output image data.

In the third embodiment of the present invention, because the image data are output in parallel from the CCD 4, the image data encoder 10 is capable of inputting the image data in parallel. The image data encoder 10 can directly execute encoding for the parallel image data, but it can also execute ordinary encoding by converting the parallel image data to serial data. In the former case, the data transfer rate to the image data encoder 10 from the CCD 4 may be increased and the encoding rate in the image data encoder 10 may also be improved. Accordingly, a high speed image processor may be realized.

The many features and advantages of the invention are apparent from the detailed specification and, thus, it is intended by the appended claims to cover all such features and advantages of the invention which fall within the true spirit and scope of the invention. Further, because numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and operation illustrated and described, and accordingly all suitable modifications and equivalents may be resorted to, falling within the scope of the invention.